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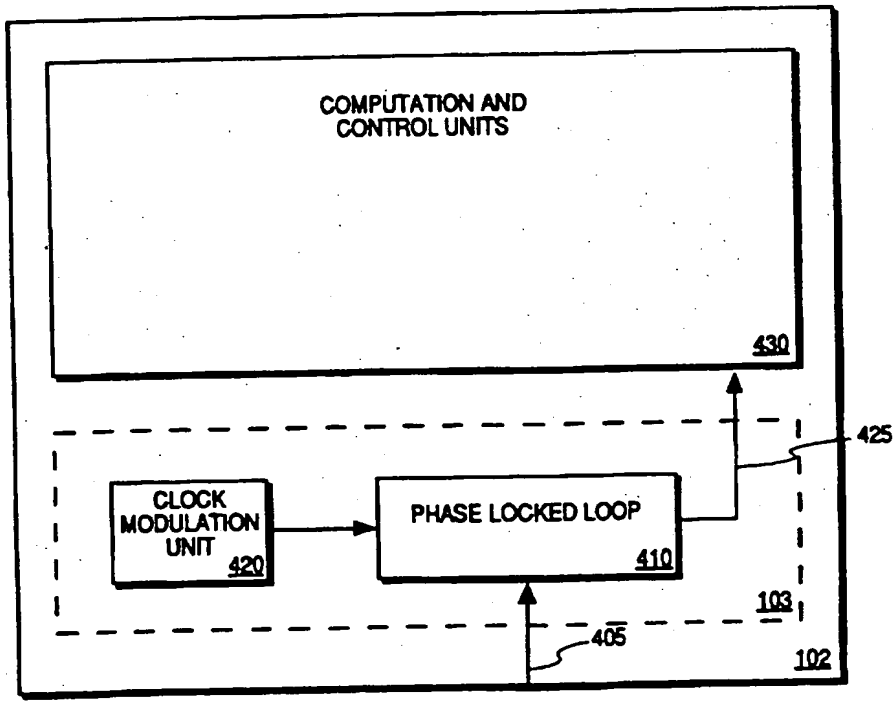

(57) Abstract

A clock apparatus (420) reduces electromagnetic emissions from a microprocessor (102). The apparatus modulates the phase locked ioop (410) of the microprocessor's internal clock so that it produces a frequency modulated ouput. The apparatus spreads the energy in the related harmonics of the internal clock over a wide band, reducing emission peaks at any given clock harmonic frequency.

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FREQUENCY MODULATED CLOCK FOR REDUCED RADIATION

FIELD OF THE INVENTION

The present invention relates to clocks in computer systems. More specifically, the present invention relates to an apparatus and method for reducing radiated emissions from microprocessors.

BACKGROUND OF THE INVENTION

Computer systems are capable of emitting electromagnetic radiation at various frequencies. Standards have been established for limiting the emission of such energy to various limits depending on the environment where the computer is used. In the past, designers of computer systems were primarily concerned with radiation emissions on the board level because radiation on the component level was fairly low and negligible. Typically, the source of the radiation from the board originated from the clock and the clock distribution system of the computer system. The radiation from these sources produced significant current levels at the clock frequency and at the harmonics of the clock.

As the development of computer systems advanced, microprocessors were designed to operate at higher frequencies in order to handle data at a higher speed. These higher operating frequencies produced greater electromagnetic radiation emission. The solutions in the prior art for minimizing radiation levels were inadequate for dealing with the radiation emissions on the component level. One approach used in the prior art to reduce the level of electromagnetic radiation in computer systems was the use of expensive metal enclosures to house the computer system. These enclosures acted as faraday cages for attenuating radiation emitted by the systems inside. Although these enclosures were effective for minimizing radiation emission in the past, these enclosures had problems attenuating radiation emitted at higher frequencies. In addition, enclosures today for portable and desktops systems are designed with lighter, less expensive materials with poorer attenuation properties. Many of these enclosures also have a greater

number of holes for additional ventilation and cable access which also contribute to poorer attenuation.

Another approach in the prior art used to reduce the level of electromagnetic radiation in computer system was the use of spread spectrum clock generators. Spread spectrum clock generators generate broadband clock frequencies. By spreading the output of the clock generator over a wide range of frequencies, the spread spectrum clock generator produced a reduced level of electromagnetic radiation. This approach was only effective for reducing emission peaks on the circuit board and from the microprocessor when the microprocessor phase locked loop bandwidth was greater than the clock modulation frequency. For a sine wave modulator, the phase locked loop of the spread spectrum clock generator required a bandwidth equal to that of the modulating frequency. This allowed tracking of the input modulation so that the output of the clock generator was modulated. For a triangle wave modulator, the phase locked loop of the spread spectrum clock generator required a bandwidth of up to ten times that of the modulating frequency. In order to reconstitute a triangle wave, the spread spectrum clock generator needed to follow up to the tenth harmonic of the triangle signal.

SUMMARY OF THE INVENTION

The present invention relates to a method and apparatus for reducing electromagnetic radiation from a microprocessor.

In one embodiment, the apparatus of the present invention includes a phase detector for comparing the frequency of an external system clock with the frequency of an internal CPU clock. The phase detector generates an analog phase error signal proportional to the phase difference. The apparatus further includes a clock modulating unit which generates a symmetrical, repetitive, varying voltage signal. The voltage signal may be one of several types including a sine wave or a triangle wave. A voltage controlled oscillator is coupled to both the phase detector and clock modulating unit. The voltage controlled oscillator generates an internal CPU clock frequency as a function of the phase error signal of the phase detector and the varying voltage signal of the

clock modulating unit. The varying voltage signal from the clock modulating unit modulates the frequency of the voltage controlled oscillator's output. This has the effect of spreading the energy in the clock related harmonics of the output over a wide band, thereby considerably reducing emission peaks at any given harmonic frequency. A line feeding back the frequency from the voltage controlled oscillator to the phase detector allows the phase detector to lock onto the input frequency of the external system clock.

The method of the present invention typically includes comparing the clock frequency of an external clock signal with that of a internal clock signal and producing voltage control signal proportional to the phase difference. After a voltage controlled signal is produced, a new internal clock signal which is a function of both the voltage control signal and a varying, clock modulating signal is generated. By generating the new internal clock signal as a function of the varying clock modulating signal, the frequency of the signal is modulated. The new internal clock signal is sent to computation and control units of the microprocessor and fed back so that its clock frequency can be compared to that of an external clock signal.

The present invention overcomes the drawbacks of the prior art by providing an apparatus and method for modulating the phase locked loop of the microprocessor's internal clock when the modulating frequency is greater than the phase locked loop bandwidth. The present invention spreads the energy in the related harmonics of the internal clock over a wide band, reducing emission peaks at any given clock harmonic frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description given below and the accompanied drawings of the preferred embodiment of the invention. The description and drawings are not meant to limit the invention to the specific embodiment. They are provided for explanation and understanding.

Figure 1 illustrates a computer system configured with the present invention.

Figure 2 illustrates the radiation emitted from clock related harmonics in a typical CPU clock.

Figure 3 illustrates the radiation emitted from a frequency modulated CPU clock.

Figure 4 illustrates a microprocessor implementing an embodiment of the present invention in block diagram form.

Figure 5 shows, in block diagram form, an embodiment of the frequency modulated CPU clock.

Figure 6 shows a schematic of one of one embodiment of the frequency modulator.

Figure 7 is a flow chart showing an embodiment of a method according to the present invention.

DETAILED DESCRIPTION

A method and apparatus for reducing electromagnetic radiation from microprocessors is disclosed. In the following description, numerous specific details are set forth to provide a thorough understanding of the present invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to obscure the present invention.

Figure 1 illustrates a computer system configured with the present invention. The computer system comprises a bus or other communication means 101 for communicating information. A microprocessor 102 is used for processing information and is coupled onto bus 101. The computer

system 100 further comprises main memory 103 coupled to bus 101. Main memory 103 is comprised of random access memory (RAM) or some other dynamic storage device which is used in storing information and instructions to be executed by microprocessor 102. Main memory 103 may also be used for storing temporary variables or other intermediate information during execution of instructions by microprocessor 102.

The computer system also comprises a read only memory (ROM) and/or other static storage devices 104 coupled to bus 101 for storing permanent information and instructions for microprocessor 102. A data storage device 105 such as a hard, floppy, or optical disk drive can be coupled to bus 101 for storing information and instructions. Also coupled to bus 101 are bus arbitrator 106 and interface/communications circuit 107. Bus arbitrator 106 is used to control the transmission and receipt of data on bus 101. Interface/communication circuit 107 is used to interface the computer system to another system, such as a computer network.

The computer system can be coupled to various devices. For example, a display device, 120, such as a cathode ray tube (CRT) can be coupled to bus 101 for displaying information to a computer user. An alphanumeric input device 121, including alphanumeric and other keys, may also be coupled to bus 101 for communicating information to the microprocessor 102. A cursor control 122 is coupled to bus 101 for communicating direction information and command selection to microprocessor 102, and for controlling cursor movement on display 120.

CPU clock 135 is inside microprocessor 102 and generates an internal clock signal used by the microprocessor 102. CPU clock 135 is coupled to an external system clock 130. CPU clock 135 receives an external clock signal from external system clock 130 and conditions this signal to meet the frequency requirement of the microprocessor 102. CPU clock 135 also modulates the buffered external clock signal from external system clock 130 to produce a frequency modulated output to computation and control units inside microprocessor 102. By modulating the output, the CPU clock 135 spreads the energy in the CPU clock

related harmonics over a wide band. This reduces the electromagnetic emission peaks at any given clock harmonic frequency.

Figure 2 illustrates the field intensity of the electromagnetic radiation generated by a typical CPU clock operating at 100 MHz. Field intensity is typically measured in decibels micro volts per meter. Energy generated from the clock is concentrated at the clock frequency's harmonics at 100 MHz, 200 MHz, 300 MHz and 1 GHz as shown by energy bands 200, 201, 202 and 203. Because the oscillator of a typical CPU clock is usually set to an exact frequency, the energy emitted at the clock's harmonics are restricted to vary narrow bands resembling spikes.

Figure 3 illustrates the field intensity of the electromagnetic radiation generated by a typical CPU clock in the prior art operating at 100 MHz 200, 201, 202, and 203 and the electromagnetic radiation generated by a CPU clock of the present invention running at the same frequency 300, 301, 302, and 303. By modulating the frequencies of the external clock signal, the CPU clock of the present invention attenuates the radiated emission amplitudes from products associated with either the clock harmonics or any signal derived from the clock signals by at least 10 dB. For regulatory measurements, the emissions are measured in a 0.1 MHz band. When the CPU clock modulates the clock frequency $\pm$ K MHz, the amplitude of the measured energy at the jth harmonic is reduced by N dB μv/m, where $N = 20 \log (jK/0.1)$.

Figure 4 illustrates a microprocessor 102 implementing an embodiment of the present invention in block diagram form. Microprocessor 102 comprises CPU clock 103 and computation and control units 430. The CPU clock 103 generates a clock signal which drives the microprocessor's computation and control units 430. Computation and control units 430 can be comprised of various components. An instruction decoder may be used in the computation and control units 410 to interpret instructions fetched from the memory 103 of the computer system. An arithmetic unit may be used to perform instructed operations such as add, complement, compare, shift, and move on quantities contained in registers. A program counter may be used to

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keep track of the current location in an executed program. Bus control circuitry could be used to handle communication with memory and I/O.

One embodiment of the CPU clock 103 comprises a phase locked loop 410 and clock modulation unit 420. Clock modulation unit 420 is coupled to phase locked loop 410. Phase locked loop 410 receives an external clock signal from input line 405 which is coupled to an external system clock. The phase locked loop 410 generates an internal clock signal which is a fixed multiple of the external clock signal. Clock modulation unit 420 may be used to modulate the phase locked loop 410 in order to modulate the frequency of the internal clock signal. By modulating the frequency of the internal clock signal, the energy in the clock related harmonics are spread over a wide band, thereby considerably reducing emission peaks at any given clock harmonic frequency. The modulated internal clock signal is sent to computation and control units 430 through output line 425.

The clock modulation unit of the present invention 420 modulates the CPU clock at a low frequency and amplitude to ensure that the maximum time variation between successive clocks does not affect CPU timing paths. As clock frequencies continue to rise on microprocessor-based systems, sources of timing variations become increasingly significant. When a microprocessor-based system is designed, a primary concern is that timing requirements are met for all device communication. The fundamental element of such communication is a clock signal that pulses at a given rate. Synchronous signals are driven and sampled at timing relative to the rising or falling edge of this clock. By modulating the frequency of the CPU clock to reduce radiation emissions, the present invention induces clock jittering which varies the clock edge of the CPU clock signal. The clock modulation unit of the present invention 420 modulates the CPU clock at a low frequency and low amplitude so that the clock jitter does not affect communication between devices within the computer system.

Consider an example where a computer system operates with a 200 MHz clock. The present invention applies a modulation that causes a 2 MHz deviation at a 50 KHz rate. This would produce a cycle-to-cycle

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variation in the clock timing from 50 nano seconds to 50.00025 nano seconds, a change of 0.25 pico seconds. Thus, timing margins needed for valid delays and setup and hold times are not reduced enough to cause miscommunication between devices.

Figure 5 illustrates an embodiment of how a clock modulation unit can be implemented with a phase locked loop. Phase locked loop 410 comprises phase detector 510, filter 520, voltage controlled oscillator 530, and a divide-by-n counter 540. Phase detector 510 is coupled to filter 520. Filter 520 is coupled to voltage controlled oscillator 530. Voltage controlled oscillator 530 is coupled to divide-by-n counter 540.

Phase detector 510 is a device that compares two input frequencies and generates a phase-error output signal that is a measure of their phase difference. A clock signal with a first frequency generated by an external system clock 130 is sent to the phase detector 510 through input line 405. Filter 520 is typically a low-pass filter which is typically used to filter out high frequency noise from the internal clock signal. Voltage controlled oscillator 530 is an oscillator whose frequency can be controlled by the phase detector output. If there is a phase difference between the two frequencies in the phase detector 510, the phase-error signal causes the voltage controlled oscillator's frequency to deviate in the direction of the first frequency. The output of the voltage controlled oscillator is sent to output line 425 and to feedback loop 535. Divide-by-n counter 540 is in feedback loop 535. Divide-by-n counter divides the output of voltage controlled oscillator by a factor of n. The resulting frequency is then sent to the phase detector 510 as the second input frequency. As a result, phase detector 510 continues to send a phase-error output signal to voltage controlled oscillator 530, causing the frequency of its output to increase until it becomes a multiple of n of the first frequency. When this occurs, the voltage controlled oscillator locks into the first frequency, maintaining a fixed phase relationship.

Clock modulation unit 420 is coupled to voltage controlled oscillator 530. Clock modulation unit 420 inputs a continuous voltage signal to voltage controlled oscillator 530 through line 525, causing it to produce a frequency modulated output. This serves to spread the energy

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in the clock related harmonics over a wide band, thereby considerably reducing emission peaks at any given clock harmonic frequency. The voltage signal from the clock modulation unit can be any symmetrical, repetitive wave form which effectively modulates the frequency of the output of the voltage controlled oscillator 530. The voltage signal can be a sine wave or a triangle wave for example. The signal is applied at a low frequency and amplitude to ensure that the maximum modulated time variation between successive clocks do not affect CPU timing paths.

The present invention modulates the internal clock signal of the microprocessor by sending a low frequency, variable voltage signal to the voltage controlled oscillator of the CPU clock's voltage controlled oscillator 530. Prior art devices, such as spread spectrum clock generators, only modulated clock frequencies external to the microprocessor. While this reduced board level radiation emitted from the external system clock and the clock distribution system, it may not reduce radiation emitted from the microprocessor's internal CPU clock. Today, it is common for internal CPU clocks to generate internal clock signals at frequencies three times the rate of the external clock signal. Future microprocessors may increase this rate to frequencies three to eight times as high. These clock frequencies emit a higher level of radiation at higher harmonics. The present invention addresses this problem by broadbanding the internal clock frequencies to reduce the electromagnetic interference at the clock's harmonic frequencies.

By modulating the internal clock signal of the microprocessor, the present invention effectively reduces electromagnetic interference at the clock's higher harmonic frequencies. This is a significant improvement over prior art solutions of using expensive metal enclosures which have problems in attenuating radiation emitted at higher frequencies.

Spread spectrum modulators in the prior art were modulated at the reference input of the phase locked loop. This imposed the constraint of having the phase locked loop bandwidth greater than the clock modulation frequency. For a sine wave modulator, the phase locked loop of the spread spectrum clock generator required a bandwidth equal to that of the modulating frequency. For a triangle wave modulator, the

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phase locked loop of the spread spectrum clock generator required a bandwidth of up to ten times that of the modulating frequency. The present invention overcomes the drawbacks of the prior art by modulating the clock at the input of voltage controlled oscillator 530.

The modulation frequency of the clock modulation unit 420 is greater than the bandwidth of the phase locked loop 410. This allows modulation to be achieved by the voltage controlled oscillator 530 without causing the phase detector 510 in the phase locked loop 410 from generating a signal in the opposite direction, canceling the modulation by the clock modulation unit 420. By using a modulation frequency greater than the bandwidth of the phase locked loop, the clock modulation unit 420 operates the voltage controlled oscillator 530 at a frequency which the phase locked loop 410 is unable to respond to.

Figure 6 illustrates a schematic of one embodiment of the clock modulation unit. In this embodiment, the clock modulation unit is a low frequency ramp generator circuit. The circuit is driven by an external clock signal, typically at a frequency in the range of 66 MHz.

Line 610 connects the clock modulation unit to an external clock signal. The external clock signal is sent to a divide-by-n counter 620 which divides the external clock signal down, typically by a factor of 1000. The clock signal is then sent to a push-pull circuit 630 through line 625. Push-pull circuit 630 is comprised of two transistors. Transistor 631 is an n-channel MOSFET. Transistor 632 is a p-channel MOSFET. The drain of transistor 631 is connected to Vcc, the system voltage. The source of transistor 631 is connected to the drain of transistor 632. The source of transistor 632 is connected to ground. External capacitor 640 is coupled to push-pull circuit 630 and to ground.

When the clock signal from line 625 is high, transistor 631 is turned on, discharging current from transistor 631 to capacitor 640. When the clock signal from line 625 is low, transistor 631 is turned off and transistor 632 is turned on, discharging current from capacitor 640 into transistor 632. Transistors 631 and 632 are sized so that they have identical on-resistance and so that transistor 632 charges the same amount of current that transistor 631 discharges. Resistors 651 and 652 attenuate and

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isolate the output signal to the voltage controlled oscillator so that the internal clock frequency is modulated appropriately.

Figure 7 illustrates, in flow chart diagram form, a method of reducing radiation emission from a microprocessor according to one embodiment of the present invention. The frequencies of an external system clock signal is compared with the frequencies of an internal clock signal generated within the microprocessor, as shown in block 710. Typically, this is done using a phase detector. Next, a voltage control signal proportional to the phase difference of the two clock signals is generated. This is shown in block 720. Next, a clock modulation signal is generated. Typically, the signal is generated by a clock modulation unit. The signal may be, for example, a continuous sine wave or a triangle wave. This is shown in block 730. Next, an internal clock signal is generated, as shown in block 740. The frequency of the signal is a function of the voltage control signal and the clock modulation signal. Typically, the internal clock signal is generated by a voltage controlled oscillator. The modulation signal modulates the frequency of the internal clock signal. This spreads the energy in the clock-related harmonics of the signal over a wide band, thereby considerably reducing emission peaks at any given clock harmonic frequency. As shown in block 750, the internal clock signal is sent to the computation and control units of the microprocessor. Next, the internal clock signal is sent a divide-by-n counter as shown in block 760. The divide-by-n counter divides the frequency of the internal clock signal by a predetermined factor. Next, the clock frequencies of an external clock signal is compared with the internal clock signal, as we return to block 710. By dividing the internal clock frequency by a predetermined factor, the clock frequencies of future internal clock signals will increase as voltage control signals are generated to indicate the phase difference of the present internal clock frequency.

If the computer system uses an internal clock that is different from the I/O clock, the I/O would be synchronized with the external clock frequency.

Thus, a method and apparatus for reducing electromagnetic emissions from a microprocessor is disclosed.

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CLAIMS

What is claimed is:

1. An apparatus for reducing electromagnetic radiation comprising:

a clock generating unit for generating an internal clock frequency for a microprocessor; and

a clock modulating unit coupled to said clock generating unit for modulating said internal clock frequency such that energy in a clock harmonic of said internal clock frequency is spread over a wide frequency range.

2. The apparatus in claim 1 wherein said clock modulating unit is a low frequency signal generator.

3. The apparatus in claim 2 wherein said low frequency signal generator generates a triangle wave signal.

4. The apparatus in claim 2 wherein said low frequency signal generator generates a sine wave signal.

5. The apparatus in claim 2 wherein said clock modulating unit produces a cycle-to-cycle variation in clock timing of less than one pico second.

6. An internal clock inside a microprocessor comprising:

a phase detector unit for comparing a frequency of an external clock signal with a frequency of an internal clock signal and for generating a voltage control signal proportional to a phase difference of said external clock signal and said internal clock signal;

a clock modulating unit for producing a low frequency voltage signal;

a voltage controlled oscillator coupled to said phase detector and said clock modulating unit for generating a new internal clock signal with

a clock frequency a function of said voltage controlled signal and said low frequency voltage signal wherein energy in a clock harmonic of said clock frequency of said new internal clock signal is spread over a wide frequency range; and

a feedback connection from said voltage controlled oscillator to said phase detector unit for allowing said new internal clock to lock onto said frequency of said external clock.

7. The internal clock in claim 6 wherein a low pass filter coupled to said phase detector filters out noise from said internal clock signal.

8. The internal clock in claim 6 wherein a divide-by-n counter coupled to said voltage controlled oscillator and said phase detector is used for generating a new internal clock signal with frequency a multiple of that of said external clock frequency.

9. The internal clock in claim 6 wherein said clock modulating unit is a signal generator generating a triangle wave signal.

10. The internal clock in claim 6 wherein said clock modulating unit is a signal generator generating a sine wave signal.

1.1. The internal clock in claim 6 wherein said clock modulating unit is a signal generator produces a cycle-to-cycle variation in clock timing of less than one pico second.

12. A computer system comprising:

a microprocessor for processing digital data;

a memory coupled to said microprocessor for storing digital data;

a display device coupled to said microprocessor for displaying information to a computer system user;

a system clock for generating an external clock signal at a first frequency; and

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an internal clock inside said microprocessor coupled to said system clock for generating an internal clock signal at a second frequency, said internal clock comprising a phase locked loop for generating an internal clock frequency and a clock modulating unit coupled to said phase locked loop for modulating said internal clock frequency such that energy in a clock harmonic of said internal clock frequency is spread over a wide frequency range.

13. The internal clock in claim 12 wherein said clock modulating unit is a low frequency signal generator.

14. The internal clock in claim 13 wherein said low frequency signal generator generates a triangle wave signal.

15. The internal clock in claim 13 wherein said low frequency signal generator generates a sine wave signal.

16. The internal clock in claim 13 wherein said clock modulating unit produces a cycle-to-cycle variation in clock timing of less than one pico second.

17. A method for reducing electromagnetic emissions from a microprocessor, said method comprising the steps of:

comparing clock frequencies of an external clock signal with that of an internal clock signal;

producing a voltage control signal proportional to a phase difference in said external clock signal and said internal clock signal;

producing a low frequency clock modulation signal; and

generating a new internal clock signal with a frequency a function of said voltage control signal and said low frequency clock modulation signal.

18. The method of claim 17 wherein said step of producing a low frequency clock modulation signal is achieved by producing a continuous, varying voltage signal.

19. The method of claim 17 wherein said comparing step is performed by a phase detector.

20. The method of claim 17 wherein said generating step is performed by a voltage controlled oscillator.

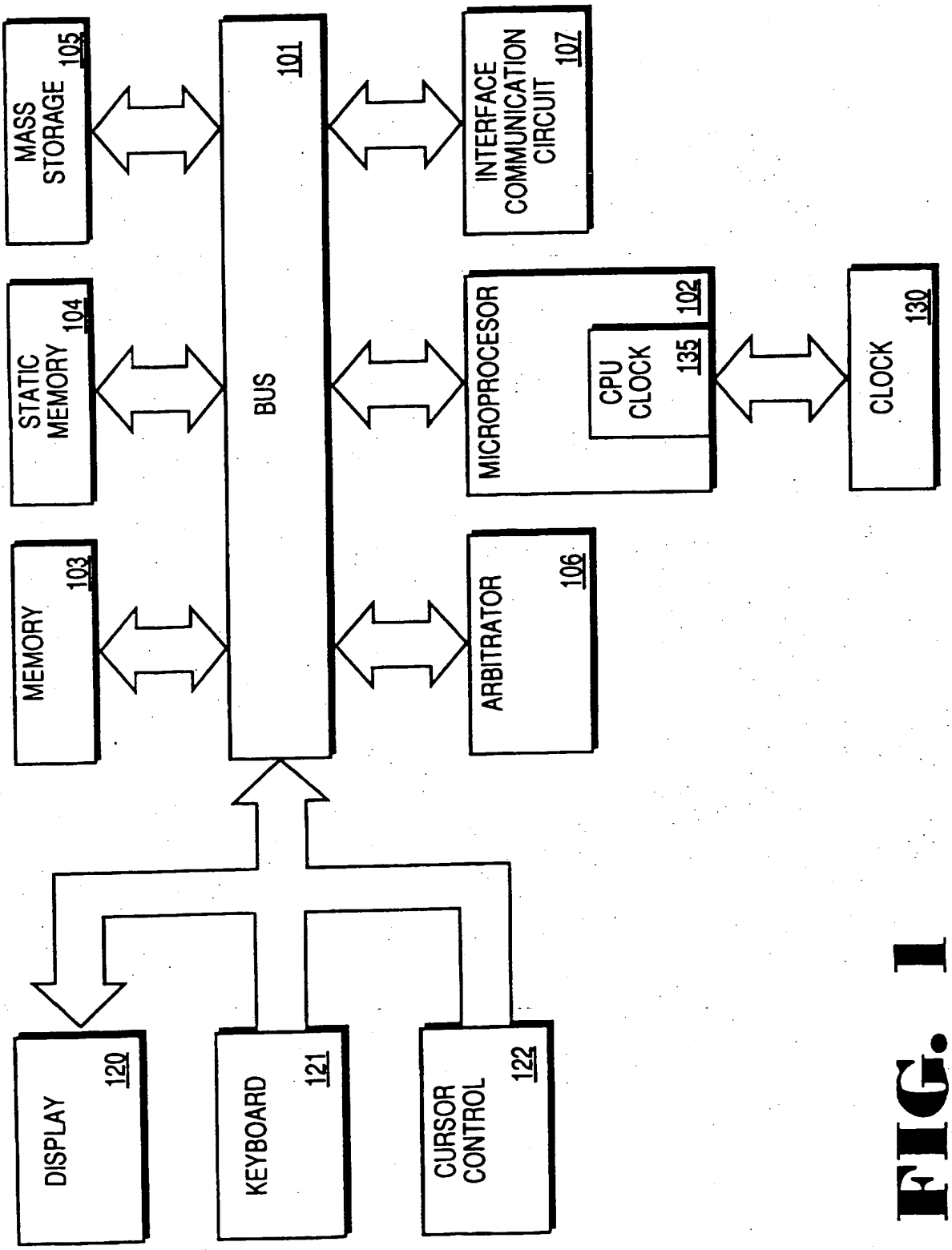

FIG. 1

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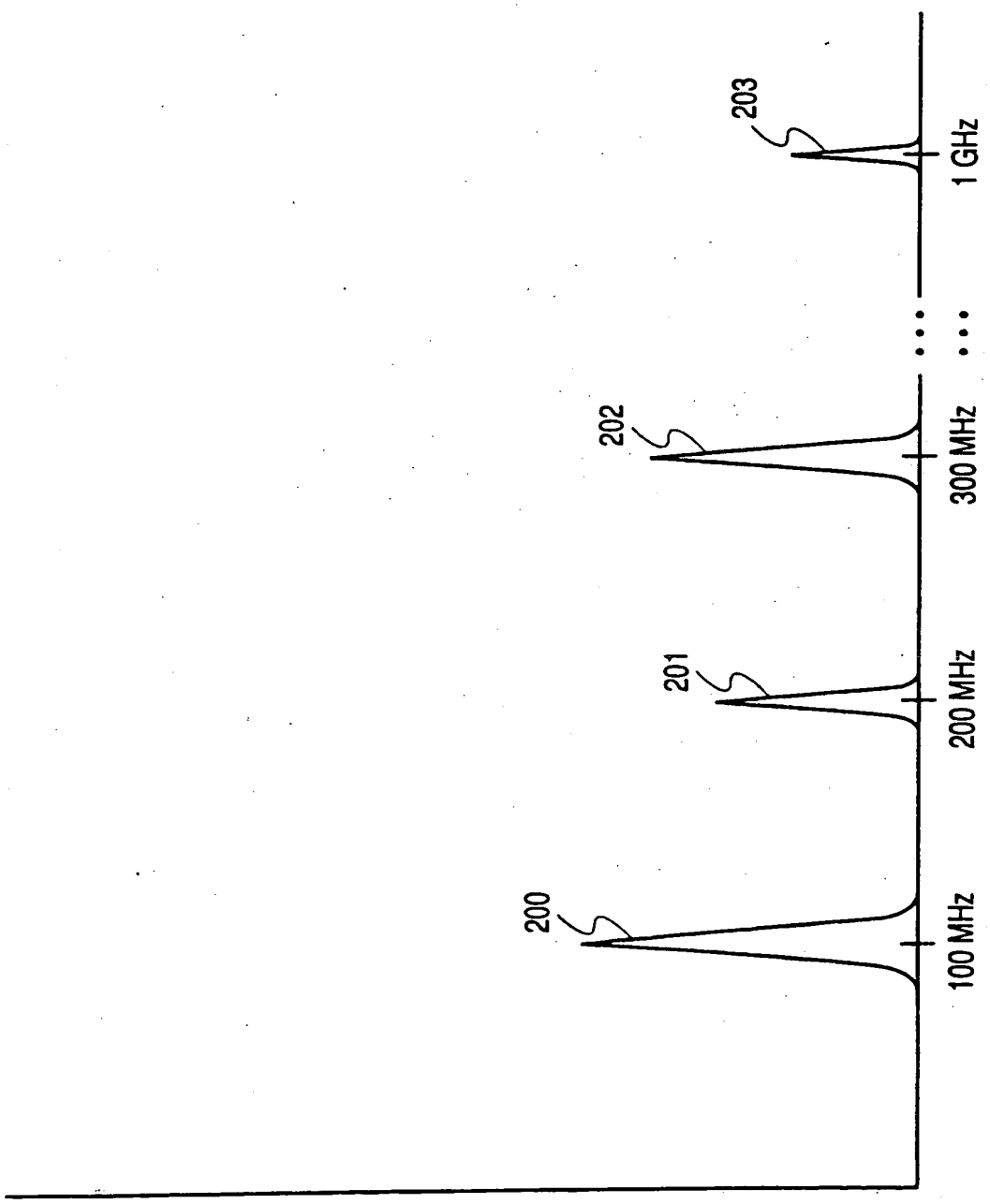

FIG. 2

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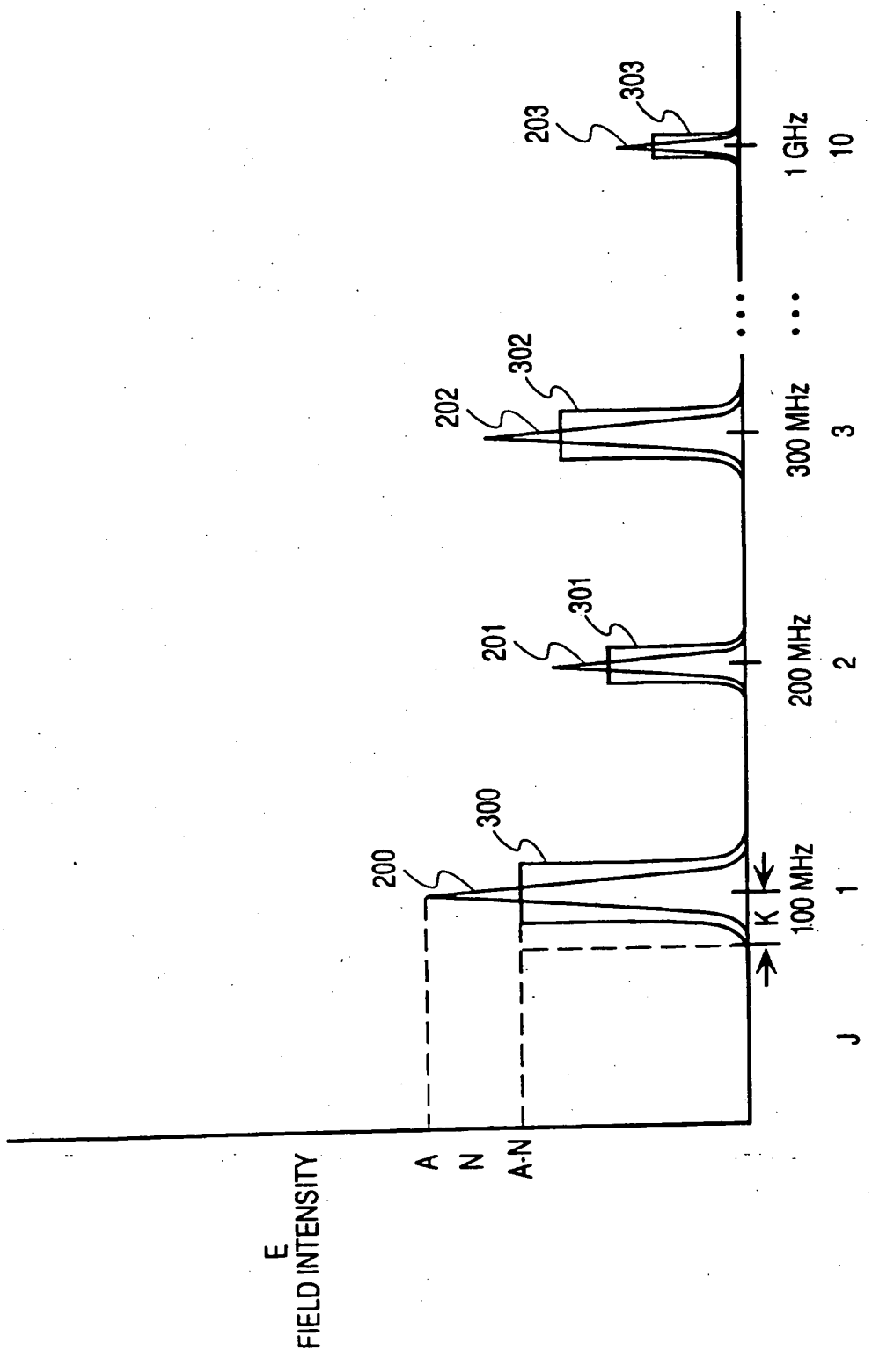
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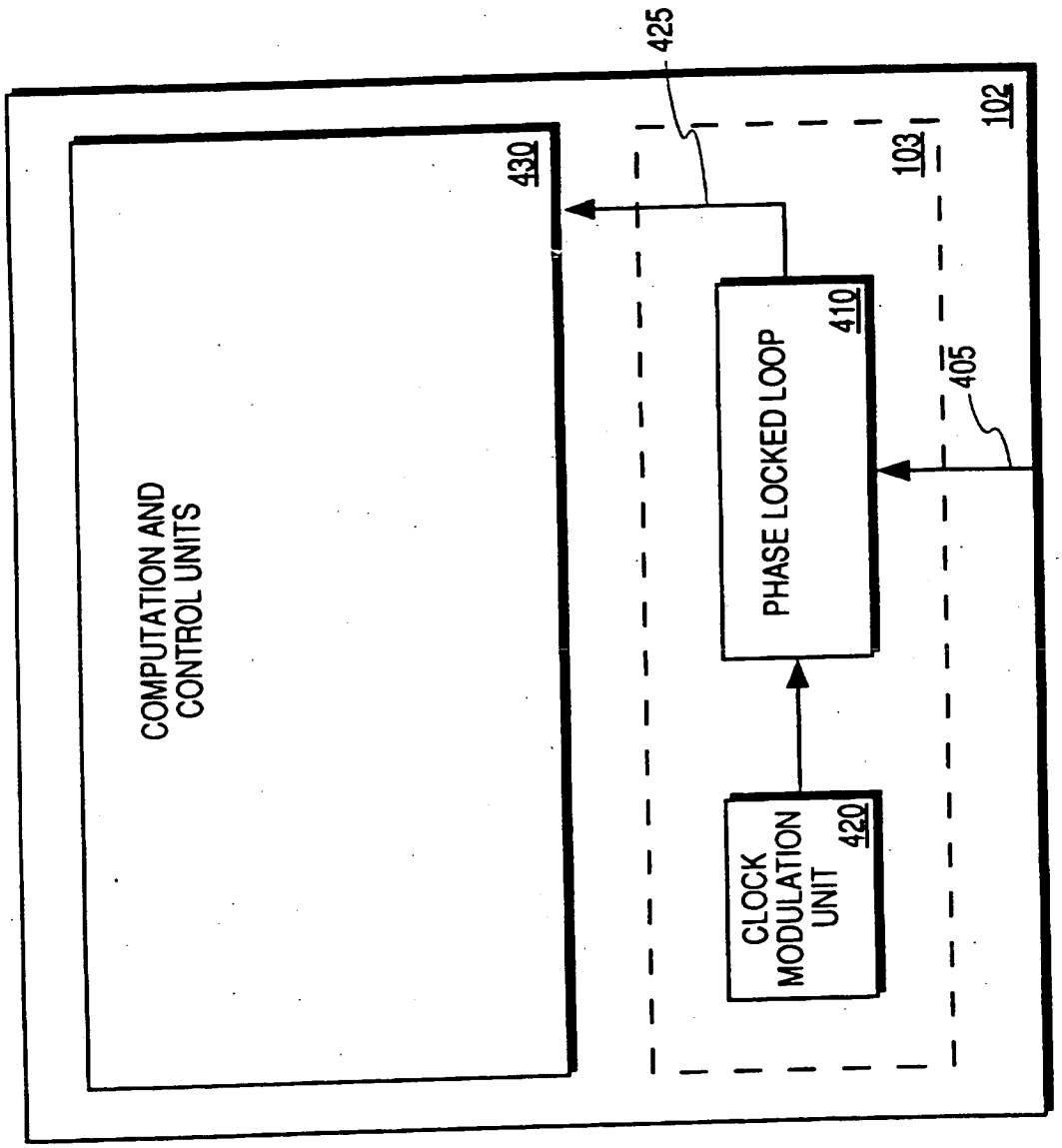
FREQUENCY

FIG. 3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102
103
430
COMPUTATION AND CONTROL UNITS
PHASE LOCKED LOOP
410
405
CLOCK MODULATION UNIT
420

FIG. 4

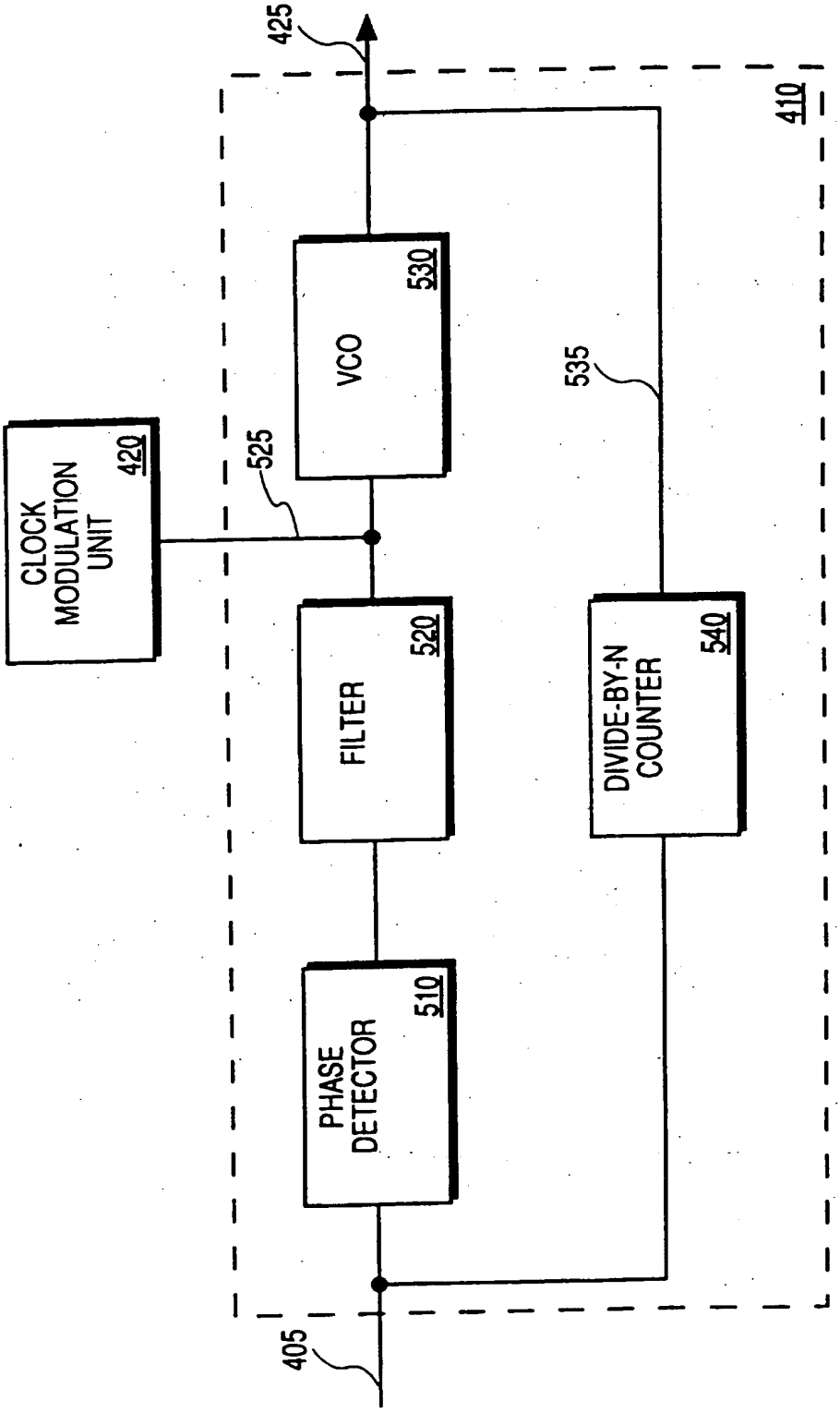

FIG. 5

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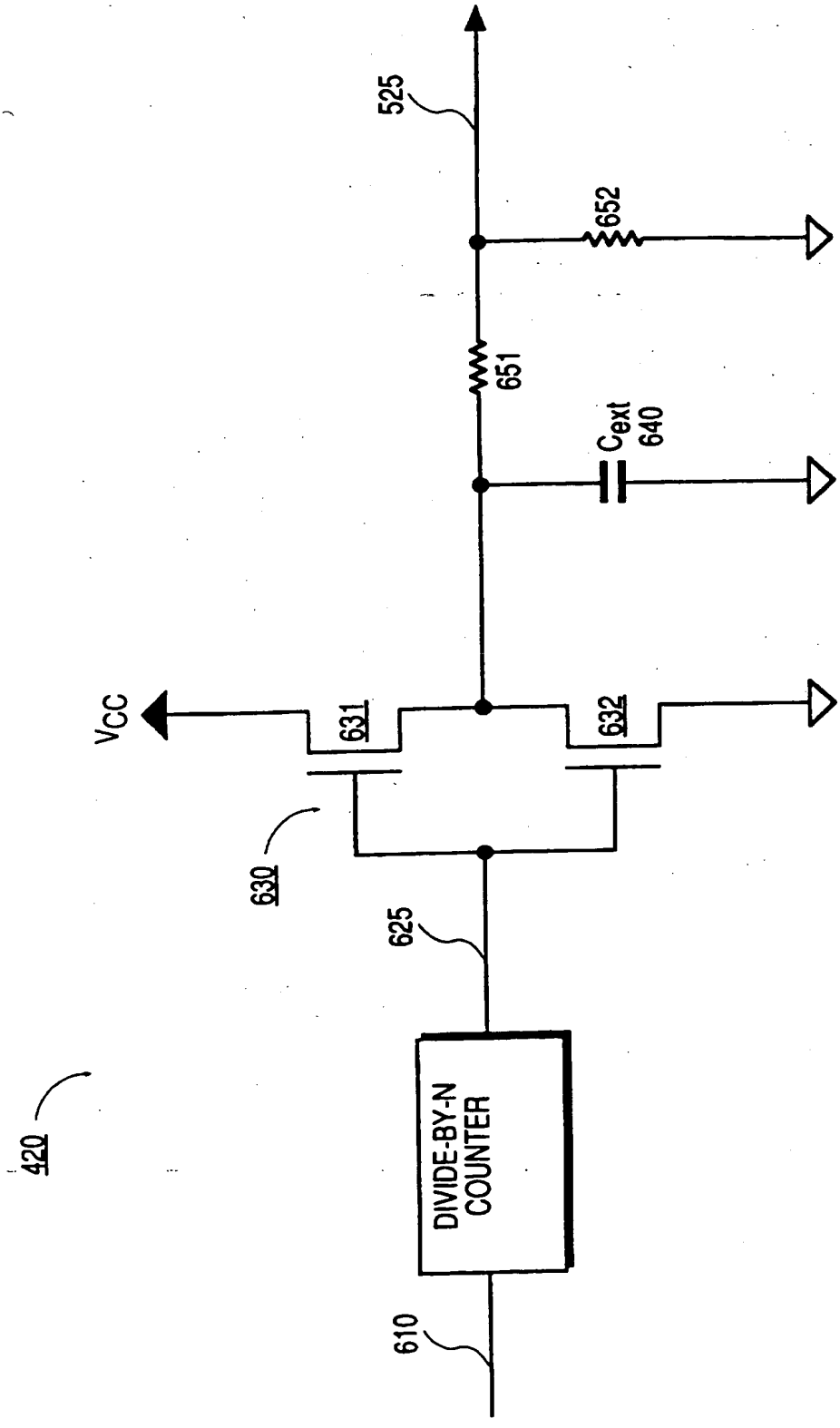

FIG. 6

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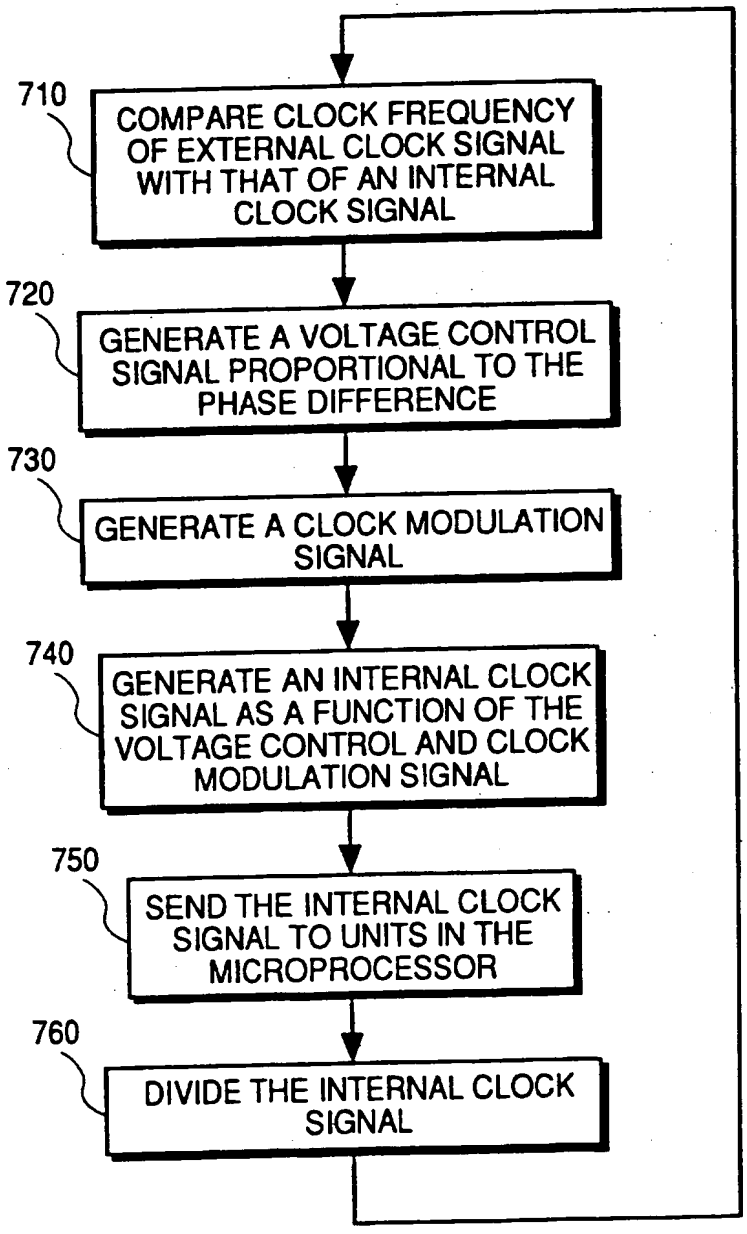

FIG. 7

BNSDOCID: <WO 9627943A1 I >

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/01426

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H03B 29/00; H04L 7/00
US CL : 331/1A, 23, 25, 78; 327/156, 164, 181, 291; 332/127; 375/376

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 331/1A, 23, 25, 78; 327/156, 164, 181, 291; 332/127; 375/376

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A,4,507,796 (STUMFALL) 26 MARCH 1985, SEE FIG.2 AND COL.4, LINES 50-62.	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search 05 APRIL 1996	Date of mailing of the international search report 24 MAY 1996
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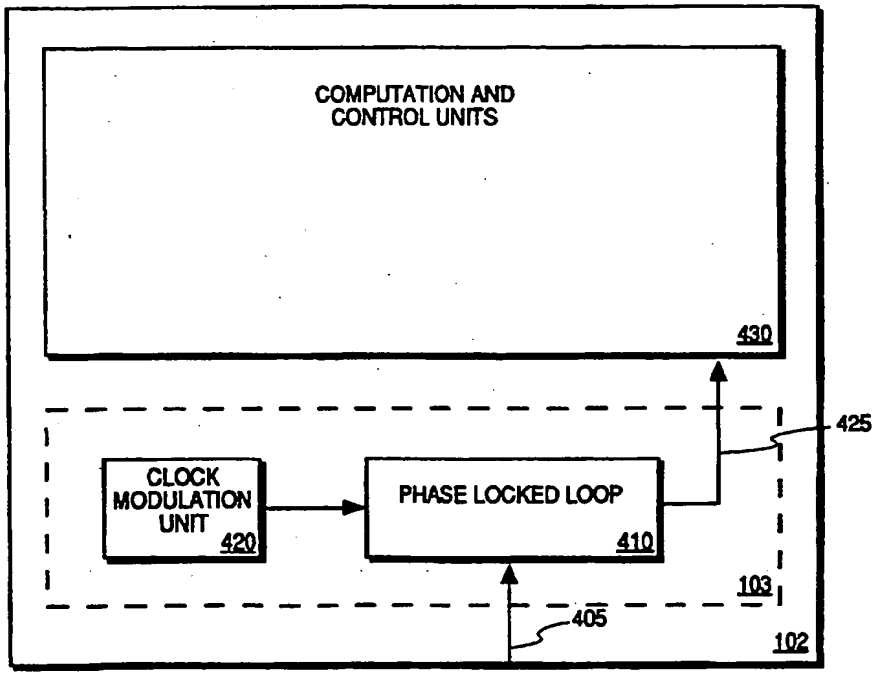
Published
With international search report.

(54) Title: FREQUENCY MODULATED CLOCK FOR REDUCED RADIATION



(57) Abstract

A clock apparatus (420) reduces electromagnetic emissions from a microprocessor (102). The apparatus modulates the phase locked loop (410) of the microprocessor's internal clock so that it produces a frequency modulated ouput. The apparatus spreads the energy in the related harmonics of the internal clock over a wide band, reducing emission peaks at any given clock harmonic frequency.

• (Referred to in PCT Gazette No. 50/1996, Section II)

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